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EXAMINER	
NORTON, JENNIFER L	

ART UNIT	PAPER NUMBER
2121	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/783,495	CHEN ET AL.	
	Examiner	Art Unit	
	Jennifer L. Norton	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a **Final Office Action** in response to the Amendment received on 27 June 2007. Claims 1, 12, 16-18, 21 and 22 been amended. Claims 1-22 are pending in this application.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4 and 9-11 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over U.S. Patent No. 5,409,538 Nakayama in view of U.S. Patent Publication No. 2004/0092047 (hereinafter Lymberopoulous).

4. As per claim 1, Nakayama teaches a method for controlling exposure energy on a wafer substrate, comprising the steps of:

controlling the exposure energy with a feedback process control signal of critical dimension (col. 6, lines 14-20 and 48-55, col. 15, lines 12-21 and Fig. 18), and

further controlling the exposure energy with a feed forward process control signal of a compensation amount that compensates for wafer thickness variations (col. 6, lines 48-55 and col. 15, lines 14-41, i.e. "the results of the correction"),

Nakayama does not expressly teach a patterned wafer substrate and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate.

Lymberopoulous teaches to a patterned wafer substrate (pg. 3, par. [0028]) and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate (pg. 1, par. [0007]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include a patterned wafer substrate and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate to provide a simple, cost-effective methodology for fast and meaningful identification and correction of CD variation without significantly compromising throughput (pg. 2, par. [0013]).

If, however the prior art is interpreted differently by a third party, the base

reference and secondary reference teach "a control signal of critical dimension" as follows:

As per claim 1, Nakayama teaches a method for controlling exposure energy on a wafer substrate, comprising the steps of:

controlling the exposure energy with a feedback process control signal (col. 6, lines 14-20 and 48-55, col. 15, lines 12-21 and Fig. 18), and

further controlling the exposure energy with a feed forward process control signal of a compensation amount that compensates for wafer thickness variations (col. 6, lines 48-55 and col. 15, lines 14-41, i.e. "the results of the correction").

Nakayama does not expressly teach a patterned wafer substrate, control signal of critical dimension and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate.

Lymberopoulous teaches to a patterned wafer substrate (pg. 3, par. [0028]), a wafer measuring tool where the CD is optically measured on a patterned photoresist layer (pg. 4, par. [0036]) and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate (pg. 1, par. [0007]).

Therefore, it would have been obvious to a person of ordinary skill in the art at

the time of applicant's invention to modify the teaching of Nakayama to include a patterned wafer substrate, a wafer measuring tool where the CD is optically measured on a patterned photoresist layer and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate to provide a simple, cost-effective methodology for fast and meaningful identification and correction of CD variation without significantly compromising throughput (pg. 2, par. [0013]).

5. As per claim 2, Nakayama teaches as set forth above combining the feed forward control signal with the feedback process control signal to control the exposure energy (col. 15, lines 14-33 and Fig. 18).

6. As per claim 3, Nakayama teaches as set forth above supplying the feed forward process control signal by a feed forward controller (col. 15, lines 21-41 and Fig. 18, element 45).

7. As per claim 4, Nakayama teaches as set forth above controlling the exposure energy by a feed forward control signal of an interlayer thickness measurement (col. 6, lines 48-55, col. 15, lines 8-28 and Fig. 18, element 56).

8. As per claim 9, Nakayama teaches as set forth above calculating the compensation amount according to a polynomial function with higher order coefficients set at zero (col. 5, lines 17-32 and 38-51).

9. As per claim 10, Nakayama teaches as set forth above calculating the compensation amount according to a linear function (col. 5, lines 38-51).

10. As per claim 11, Nakayama teaches as set forth above calculating the compensation amount according to a segmented linear function (col. 5, lines 17-32 and 38-51).

11. Claims 5-8 and 12-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakayama in view of Lymberopoulous in further view of Saka.

12. As per claim 5, Nakayama teaches as set forth above controlling the exposure energy by a feed forward control signal of an interlayer thickness measurement (col. 15, lines 8-28 and Fig. 18, element 56).

Nakayama nor Lymberopoulous expressly teach an interlayer thickness measurement remaining after chemical mechanical planarization.

Saka teaches to an interlayer thickness measurement remaining after chemical mechanical planarization (col. 8, lines 61-63 and col. 13, lines 27-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include an interlayer thickness measurement remaining after chemical mechanical planarization to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

13. As per claim 6, Nakayama teaches as set forth above calculating the compensation amount according to a polynomial function with a coefficient of the function being based on a measurement of a thickness of a planarized interlayer (col. 6, lines 35-55 and col. 15, lines 17-33).

Nakayama nor Lymberopoulous expressly teach a measurement of a remaining thickness of a planarized interlayer.

Saka teaches to a measurement of a remaining thickness of a planarized interlayer (col. 8, lines 61-63 and col. 13, lines 27-33).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include a measurement of a remaining thickness of a planarized interlayer to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

14. As per claim 7, Nakayama teaches as set forth above to calculating the feedback process control signal of critical dimension measurement of a layer (col. 6, lines 48-55, col. 15, lines 21-33 and Fig. 18)

Nakayama nor Lymberopoulous expressly teach calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot.

Saka teaches to calculating the feedback process control signal of critical dimension measurement of a top layer in a previous manufacturing lot (col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include calculating the feedback process control signal of critical

dimension measurement of a top layer in a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the critical dimension process (col. 5, lines 38-40).

15. As per claim 8, Nakayama teaches as set forth above to calculating the compensation amount according to a polynomial function with a coefficient of the function being based on a measurement of a remaining thickness of a planarized interlayer (col. 6, lines 48-55) and calculating the feedback process control signal of critical dimension measurement of a layer (col. 15, lines 17-33).

Nakayama nor Lymberopoulous expressly teach a critical dimension measurement of a top layer in a previous manufacturing lot.

Saka teaches to a critical dimension measurement of a top layer in a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include a critical dimension measurement of a top layer in a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the critical dimension process (col. 5, lines 38-40).

16. As per claim 12, Nakayama teaches a system for controlling exposure energy on a first wafer substrate, comprising:

a feed forward controller (Fig. 18, element 45) providing a feed forward control signal to an exposure apparatus based on a thickness measurement of an interlayer of the first wafer substrate for controlling the exposure energy focused on a top layer of the first wafer substrate (col. 15, lines 14-41), and

a feedback controller (Fig. 18, element 45) providing a feedback exposure energy control signal to the exposure apparatus based on critical dimension measurement of a layer of a wafer substrate (col. 15, lines 17-33).

Nakayama does not expressly teach a patterned wafer substrate, a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot, the critical dimension being one of a width, a spacing and an opening of the second patterned wafer substrate.

Lymberopoulous teaches to a patterned wafer substrate (pg. 3, par. [0028]) and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate (pg. 1, par. [0007]).

Lymberopoulous does not expressly teach a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot.

Saka teaches to a critical dimension measurement of a top layer of a second wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include a patterned wafer substrate and critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate to provide a simple, cost-effective methodology for fast and meaningful identification and correction of CD variation without significantly compromising throughput (Lymberopoulous: pg. 2, par. [0013]); and a critical dimension measurement of a top layer of a second wafer substrate of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (Saka: col. 5, lines 38-40).

If, however the prior art is interpreted differently by a third party, the base reference and secondary reference teach "a control signal of critical dimension" as follows:

As per claim 12, Nakayama teaches a system for controlling exposure energy on a first wafer substrate, comprising:

a feed forward controller (Fig. 18, element 45) providing a feed forward control signal to an exposure apparatus based on a thickness measurement of an interlayer of the first wafer substrate for controlling the exposure energy focused on a top layer of the first wafer substrate (col. 15, lines 14-41), and

a feedback controller (Fig. 18, element 45) providing a feedback exposure energy control signal to the exposure apparatus based on a measurement of a layer of a wafer substrate (col. 15, lines 17-33).

Nakayama does not expressly teach a patterned wafer substrate, a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot and the critical dimension being one of a width, a spacing and an opening of the second patterned wafer substrate

Lymberopoulous teaches to a patterned wafer substrate (pg. 3, par. [0028]), a wafer measuring tool where the CD is optically measured on a patterned photoresist layer (pg. 4, par. [0036]) and the critical dimension being one of a width, a spacing and an opening of a wafer substrate (pg. 1, par. [0007]).

Lymberopoulous does not expressly teach a critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot.

Saka teaches to a critical dimension measurement of a top layer of a second wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama to include a patterned wafer substrate, a wafer measuring tool where the CD is optically measured on a patterned photoresist layer and the critical dimension being one of a width, a spacing and an opening of a wafer substrate to provide a simple, cost-effective methodology for fast and meaningful identification and correction of CD variation without significantly compromising throughput (Lymberopoulous: pg. 2, par. [0013]); and a critical dimension measurement of a top layer of a second wafer substrate of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (Saka: col. 5, lines 38-40).

17. As per claim 13, Nakayama teaches as set forth above a thickness measurement device (Fig. 18, element 56) providing thickness measurement data to the feed forward controller (col. 15, lines 8-28 and Fig. 18, element 45).

18. As per claim 14, Nakayama teaches as set forth above a critical dimension measurement device (Fig. 18, element 56) providing critical dimension measurement data to the feedback controller (Fig. 18, element 45 and col. 15, lines 8-28).

19. As per claim 15, Nakayama teaches as set forth above a thickness measurement device (Fig. 18, element 56) providing thickness measurement data to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-28) and a critical dimension measurement device (Fig. 18, element 56) providing critical dimension measurement data to the feedback controller (Fig. 18, element 45 and col. 15, lines 8-28).

20. As per claim 16, Nakayama teaches as set forth above a thickness measurement device (Fig. 18, element 56) providing thickness measurement data of a shallow trench isolation layer of the first patterned wafer substrate to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-28).

21. As per claim 17, Nakayama teaches as set forth above a critical dimension measurement device (Fig. 18, element 56) providing critical dimension measurement data of a poly-gate of the wafer substrate (col. 15, lines 8-17).

Nakayama nor Lymberopoulous expressly teaches as set forth

above to critical dimension measurement data of a poly-gate of the second patterned wafer substrate of a previous manufacturing lot.

Saka teaches to critical dimension measurement data of a poly-gate of the second patterned wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include critical dimension measurement data of a poly-gate of the second patterned wafer substrate of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

22. As per claim 18, Nakayama teaches as set forth above to a thickness measurement device providing thickness measurement data of a shallow trench isolation layer of the first patterned wafer substrate to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-17); and

a critical dimension measurement device (Fig. 18, element 56) providing critical dimension measurement data of a poly-gate (col. 15, lines 8-17).

Nakayama nor Lymberopoulous expressly teach to critical dimension measurement data of a poly-gate of a previous manufacturing lot.

Saka teaches to critical dimension measurement data of a poly-gate of wafer substrates of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include critical dimension measurement data of a poly-gate of wafer substrates of a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

23. As per claim 19, Nakayama teaches as set forth above the feed forward controller is user configurable by having one or more polynomial coefficients set to zero in a polynomial function model (col. 5, lines 12-33 and 38-51).

24. As per claim 20, Nakayama teaches as set forth above the feed forward controller is user configurable by having one or more polynomial coefficients set to zero in a polynomial function model (col. 5, lines 12-33 and 38-51).

25. As per claim 21, Nakayama teaches as set forth above a system as set forth above, comprising:

a thickness measurement device (Fig. 18, element 56) providing thickness measurement data of a shallow trench isolation layer of the first patterned wafer substrate to the feed forward controller (Fig. 18, element 45 and col. 15, lines 8-28).

26. As per claim 22, Nakayama teaches as set forth above a critical dimension measurement device (Fig. 18, element 56) providing critical dimension measurement data of a poly-gate of the wafer substrate (col. 15, lines 8-28).

Nakayama nor Lymberopoulous expressly teach to measurement data of a poly-gate of the second patterned wafer substrate a previous manufacturing lot.

Saka teaches to critical dimension measurement data (Fig .6) of a poly-gate of the second patterned wafer substrate (col. 12, lines 25-28 and col. 33, lines 4-5) of a previous manufacturing lot (col. 6, lines 58-60, col. 9, lines 28-33 and col. 12, lines 32-35).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the teaching of Nakayama in view of Lymberopoulous to include measurement data of a poly-gate of the second patterned

wafer substrate a previous manufacturing lot to continuously and in-situ, monitor localized regions of a wafer surface during the chemical mechanical planarization process (col. 5, lines 38-40).

Response to Arguments

27. Applicant's arguments see Remarks pgs. 6-7, filed 27 June 2007 with respect to claims 1-4 and 9-11 under 35 U.S.C. 102(b) have been fully considered but they are not persuasive.

28. With respect to claim 1, the Examiner emphasizes that all anticipated components and limitations of pending claims are present in the prior art. In addition, the Examiner notes the limitations of "a patterned wafer substrate" and "... controlling the exposure energy with a feedback process control signal of critical dimension...the critical dimension being one of a width, a spacing and an opening of the patterned wafer substrate" was newly presented in the Amendment After Non-Final received on 27 June 2007 by the Office, and has been addressed as set forth in the Final Office Action above.

Applicant further argues that the prior art fails to teach, "feedback or feedforward signals based on any critical dimension measurements" and "controlling the

exposure energy with a process feedback process control of critical dimension". The Examiner respectfully disagrees.

Nakayama discloses, (col. 15, lines 12-21) "The data sent from the optical property measuring system 108 is used to correct the data sent from the optical property measuring system 56. Based on the results of correction, the process controlling system 45 calculates the optimum exposure energy as a process variable for the exposure step and also calculate variations in process conditions for the photoresist coating step."

(col. 15, lines 27-41) "Then, exposure is carried out for the optimum exposure time, whereby stabilization of pattern size is contrived. The variations in process conditions for the photoresist coating step obtained by the process controlling system 45 are fed back through an interface 102 to the photoresist coating machine 49, in order to stabilize the photoresist coating and baking conditions.

In this embodiment, the optical property measuring system 108 and the optical property measuring system 56 can be connected to a plurality of photoresist coating machines to stabilize the photoresist coating and baking conditions constituting the production process conditions, and to a plurality of projection aligners fed with wafers for which the optimum exposure energy has been determined."

In summary, Nakayama discloses the feed forward process control, by using "the results of correction" (i.e. a compensation value determined based on the measured value outputted from the system) to calculate the optimum energy in process controlling system 45 to drive the system to a desired response; and the feedback process control process, by using the interface to send variations in the process back to the photoresist coating machine to stabilize its coating and baking conditions. Hence, Applicant's claimed limitations are meet as set forth above.

29. Applicant's arguments see Remarks pgs. 7-11, filed 27 June 2007 with respect to claims 5-8 and 12-22 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive.

30. With respect to claim 5-8, Applicant's argument that the prior art does not teach "controlling the exposure energy with a feedback process control signal of critical dimension", the Examiner recognizes the Applicant has not accounted for the combination of Nakayama and Saka under 35 U.S.C 103(a) for this limitation as set forth in the Non-Final Office Action mailed on 26 March 2007. The Examiner refers to the above response of pgs. 18-20, paragraph 20 of this Final Office Action and the argument, as herein addressed.

31. With respect to claim 12, the Examiner emphasizes that all anticipated components and limitations of the pending claim is present in the prior art as cited in the above 35 U.S.C 103(a) rejection of claim 12. In addition, the Examiner notes the limitation of "a feedback controller providing a feedback exposure energy control signal to the signal to the exposure apparatus based on critical dimension measurement of a top layer of a second patterned wafer substrate of a previous manufacturing lot, the critical dimension being one of a width, a spacing and an opening of the second pattered wafer substrate" was newly presented in the Amendment After Non-Final received on 27 June 2007 by the Office, and has been addressed as set forth above.

32. In regards to the Applicant's statement (pg. 8, par. 4), "**As conceded by the Action**, "Nakayama does not expressly teach a control signal of critical dimension""; the Examiner respectfully disagrees.

The Examiner recognizes the Applicant has not accounted for the rejection of claims 1 as being rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Lymberopoulous, and the rejection of claim 12 as being rejected under 35 U.S.C. 103(a) for this limitation as set forth in the Non-Office Action, mailed on 26 March 2007. The Examiner emphasizes that all anticipated components and limitations of pending claims are present in the prior art as set forth in the Non-Final Office Action mailed on 26 March 2007.

Furthermore, Nakayama discloses, (col. 6, lines 14-20) "In order to provide the exposure time thus determined, a controlling system 4 controls the illuminance of a mercury vapor lamp through power source control 2 in the illumination system and the opening and closing time of the shutter 5, whereby the pattern drawn on the reticle 7 is projected on the wafer 18 for the optimum exposure time."

(col. 6, lines 48-55) "According to this embodiment, variations in the thickness of photoresist film and variations in optical property, such as absorption coefficient, due to variations in the process conditions in the photoresist coating process can be reduced, and the photoresist coating process can be stabilized. Consequently, uniform exposure can be achieved for wafers stabilized in the photoresist coating process."

(col. 15, lines 12-21) "The data sent from the optical property measuring system 108 is used to correct the data sent from the optical property measuring system 56. Based on the results of correction, the process controlling system 45 calculates the optimum exposure energy as a process variable for the exposure step and also calculate variations in process conditions for the photoresist coating step."

(col. 15, lines 27-41) "Then, exposure is carried out for the optimum exposure time, whereby stabilization of pattern size is contrived. The variations in process conditions for the photoresist coating step obtained by the process controlling system

45 are fed back through an interface 102 to the photoresist coating machine 49, in order to stabilize the photoresist coating and baking conditions.

In this embodiment, the optical property measuring system 108 and the optical property measuring system 56 can be connected to a plurality of photoresist coating machines to stabilize the photoresist coating and baking conditions constituting the production process conditions, and to a plurality of projection aligners fed with wafers for which the optimum exposure energy has been determined."

In summary, Nakayama discloses the feed forward process control, by using "the results of correction" (i.e. a compensation value determined based on the measured value outputted from the system) to calculate the optimum energy in process controlling system 45 to drive the system to a desired response (i.e. controlling thickness), and the feedback process control process, by using the interface to send variations in the process back to the photoresist coating machine to stabilize its coating and baking conditions. Hence, Applicant's claimed limitations are meet as set forth above.

33. In regards to Applicant's argument that that Lymberopoulous does not disclose, "controlling the exposure energy with a feedback process control of critical dimension", the Examiner recognizes the Applicant has not accounted for the combination of Nakayama and Lymberopoulous under 35 U.S.C 103(a) for this limitation

as set forth in the Non-Final Office Action, mailed on 26 March 2007.

34. Claims 5-8 and 12-22 stand rejected under 35 U.S.C 103(a) as set forth above.

Conclusion

35. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer L. Norton whose telephone number is 571-272-3694. The examiner can normally be reached on 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Anthony Knight can be reached on 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Anthony Knight
Supervisory Patent Examiner
Art Unit 2121